IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Confirmation No: 4931

Yasurou MATSUZAKI Art Unit: 2819

Serial No.: 10/003,048 Examiner: Vibol Tan

Filed: December 6, 2001 Docket. No.: 108397-00052

For: INPUT/OUTPUT INTERFACE AND SEMICONDUCTOR INTEGRATED CIRCUIT HAVING INPUT/OUTPUT INTERFACE

S/A Amdt 5.8.03 Amdt

RESPONSE (AMENDMENT) UNDER 37 CFR §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 5, 2003

Sir:

In response to the outstanding Office Action dated February 3, 2003, (hereinafter "outstanding Action"), with the response having been duly submitted (May 3, 2003 being a Saturday and May 4, 2003 being a Sunday), please amend the application as follows:

IN THE CLAIMS:

Please amend claims 35 and 36 as follows:

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35. (Amended) A semiconductor integrated circuit comprising:

a transmitting circuit for converting a logical value to a predetermined delay time in accordance with the logical value, the logical value being expressed with a plurality of bits, and for outputting a transmission signal, which is behind a standard timing signal by the delay time, to a signal line.